FEA Heat Sink Analysis

Abhishek Joshi

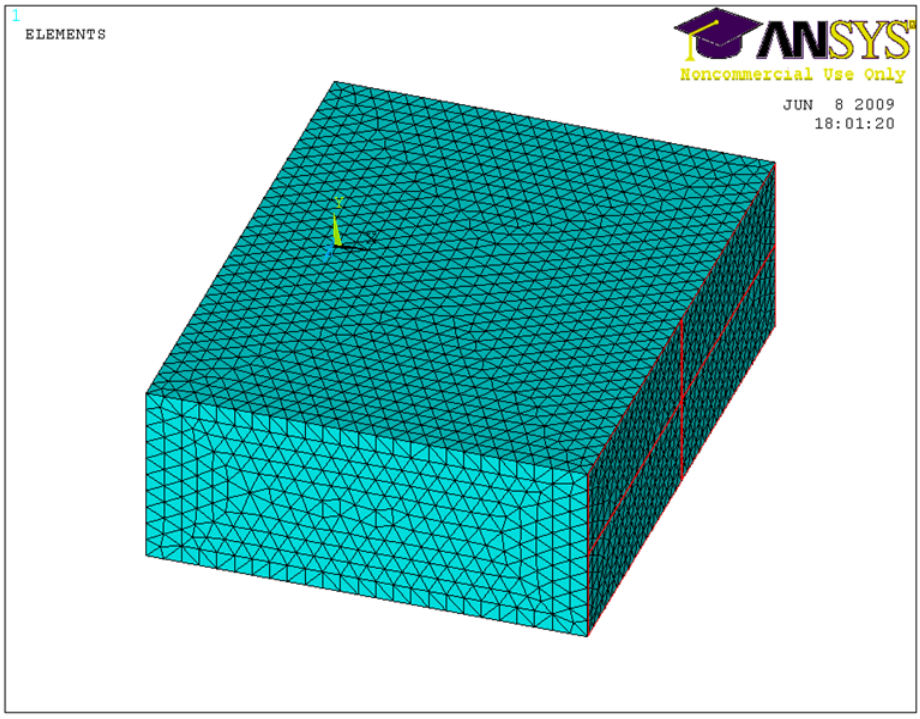

Figure 1-FE Model for Thermal Analysis of Electronic Chip and the Housing Assembly

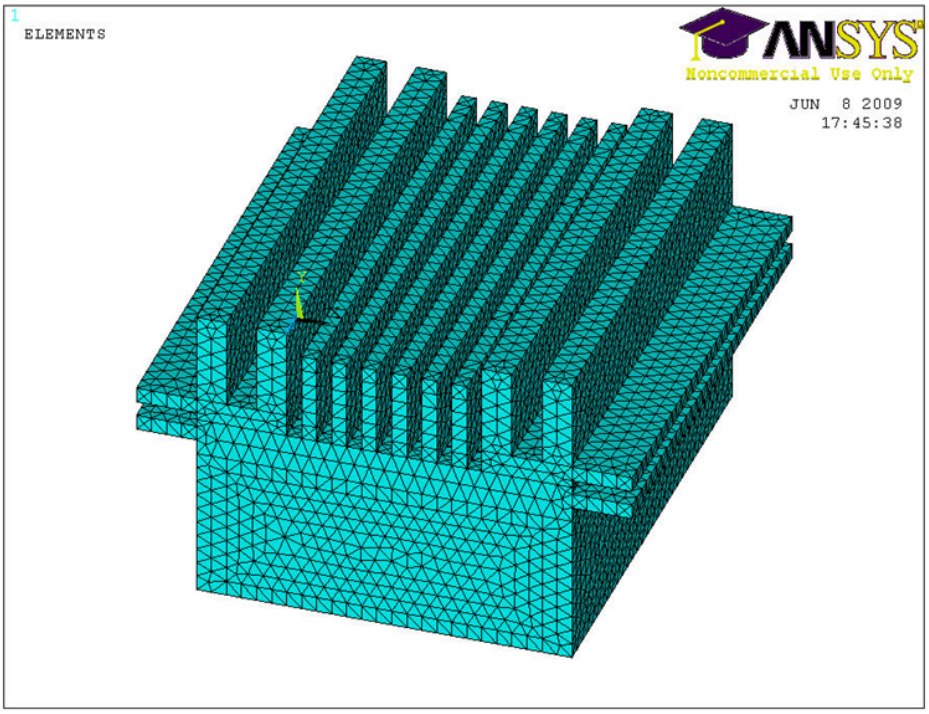

Figure 2-FE Model for Iteration Two

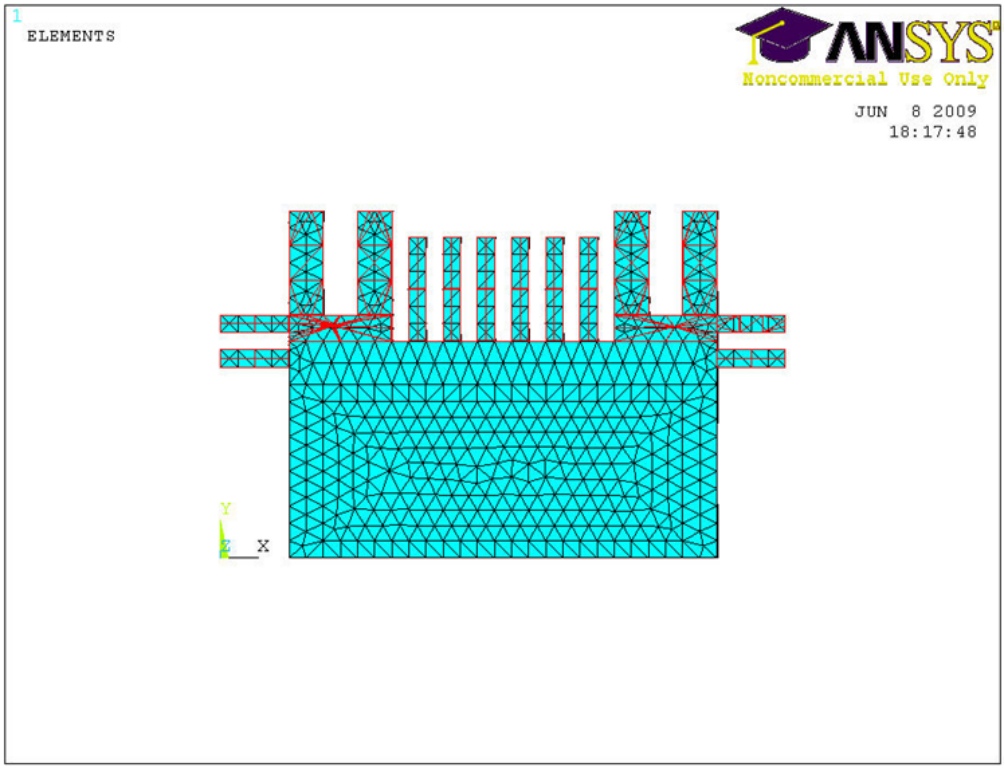

Figure 3-Convection Applied to the Fins

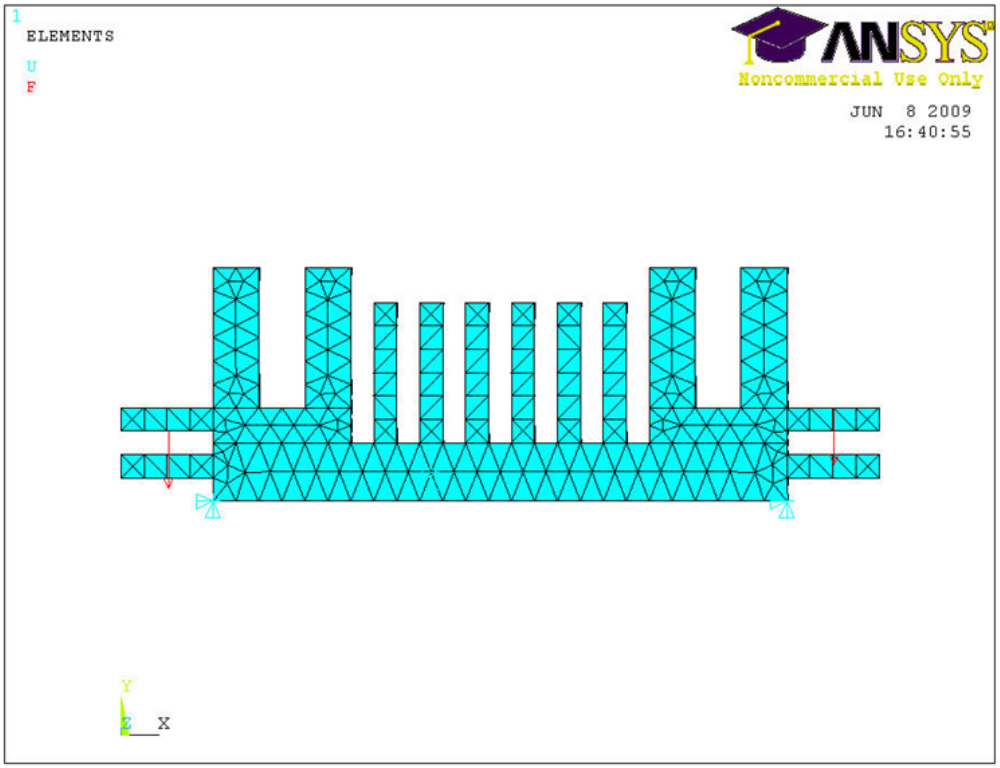

Figure 4-FE Model for Static Analysis of the Heat Sink

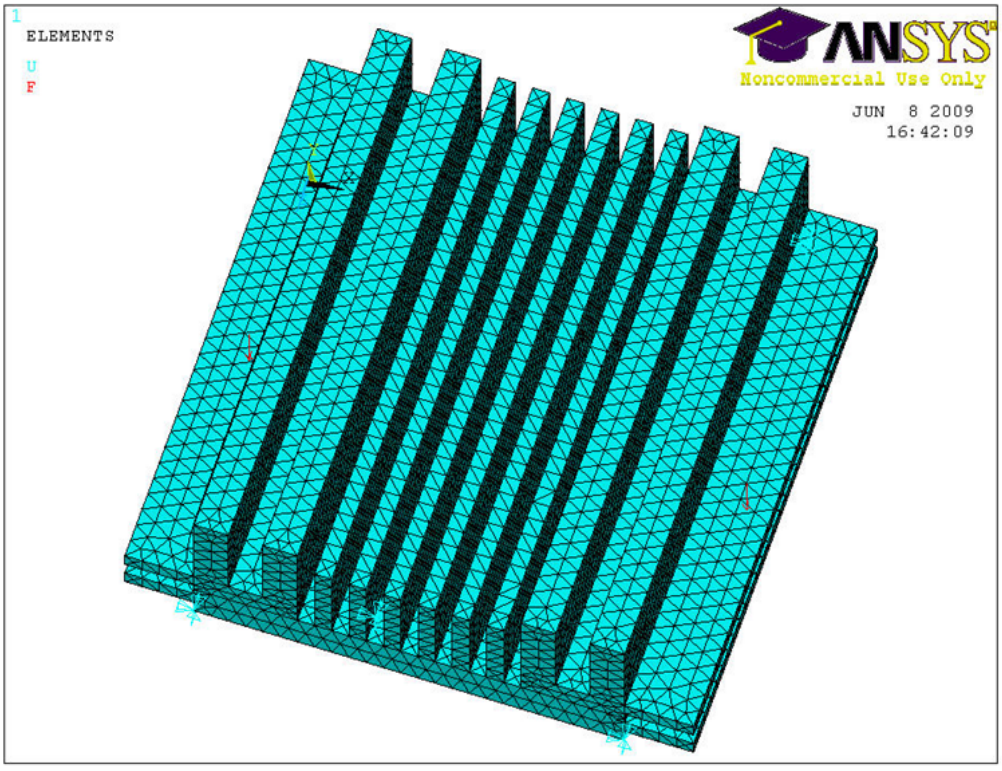

Figure 5-Top View of the Static Analysis of Heat Sink

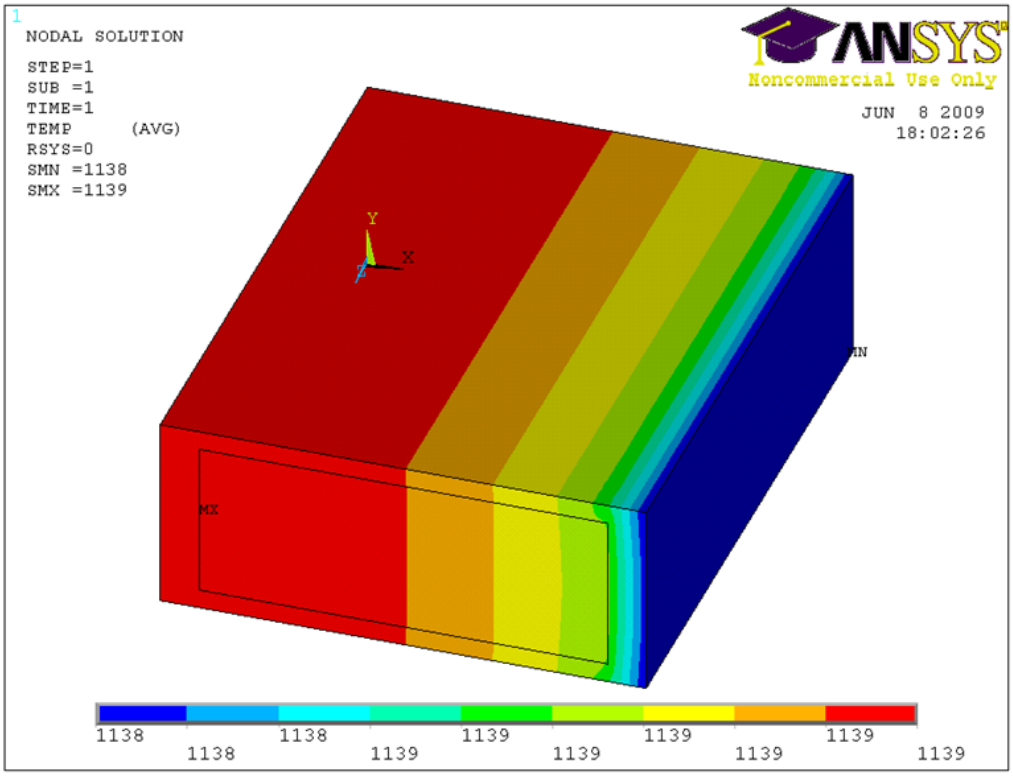

Figure 6-Thermal Analysis of the Electronic Chip and Housing Assembly

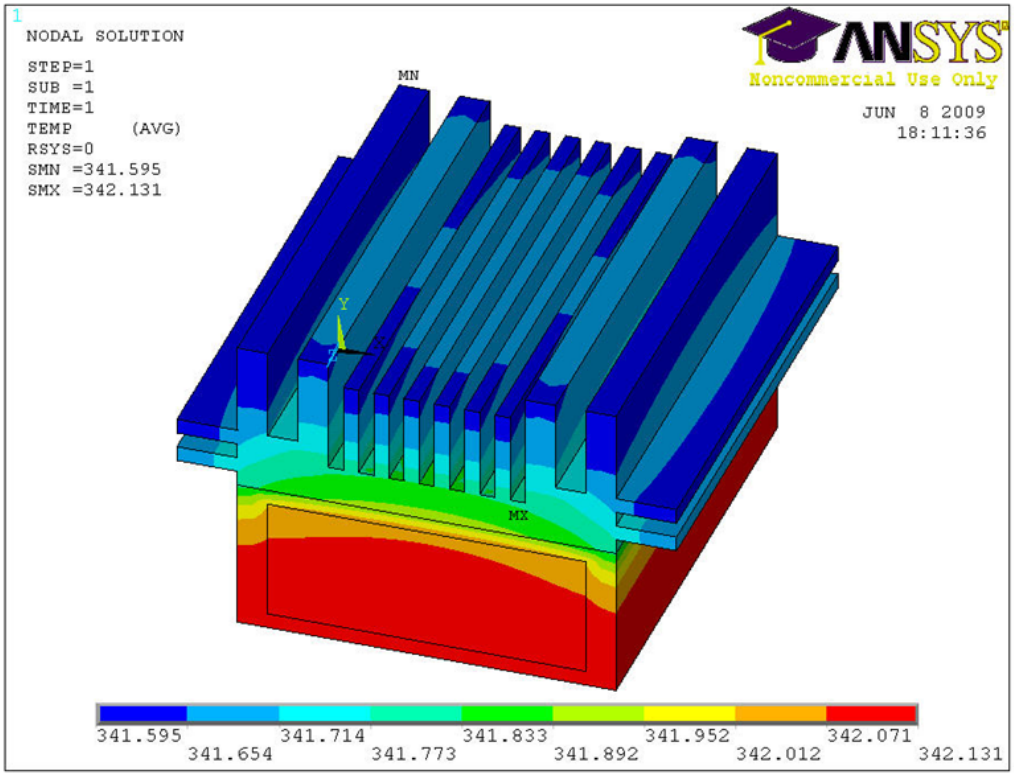

Figure 7-Heat Sink Impact

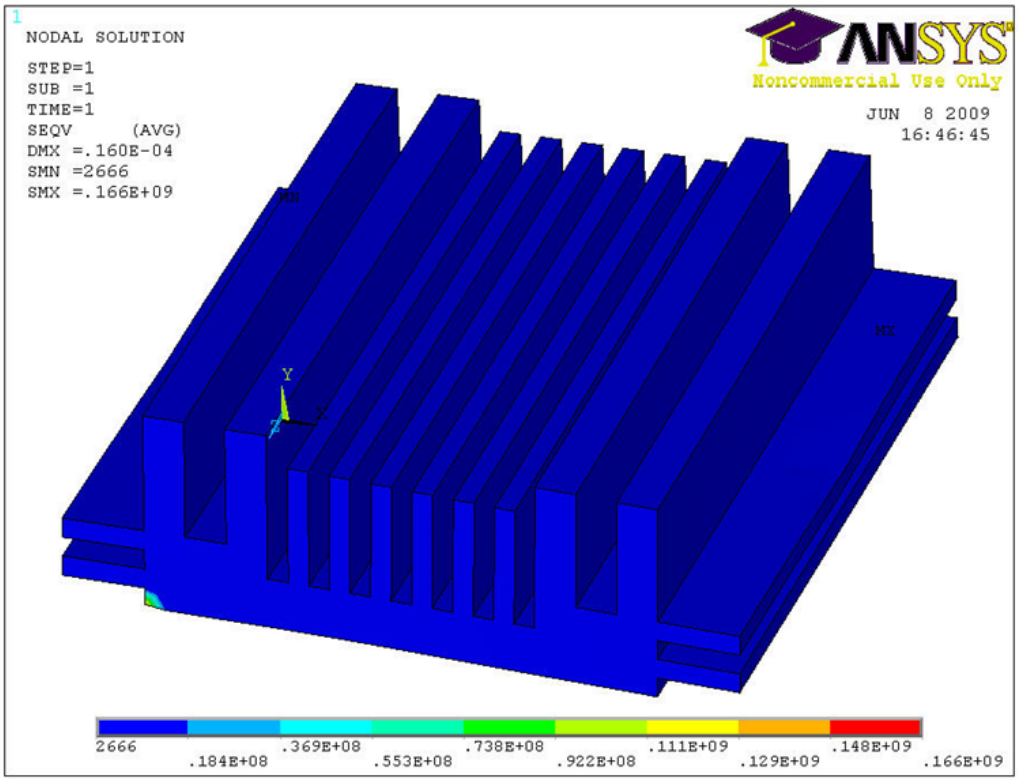

Figure 8-Static Analysis

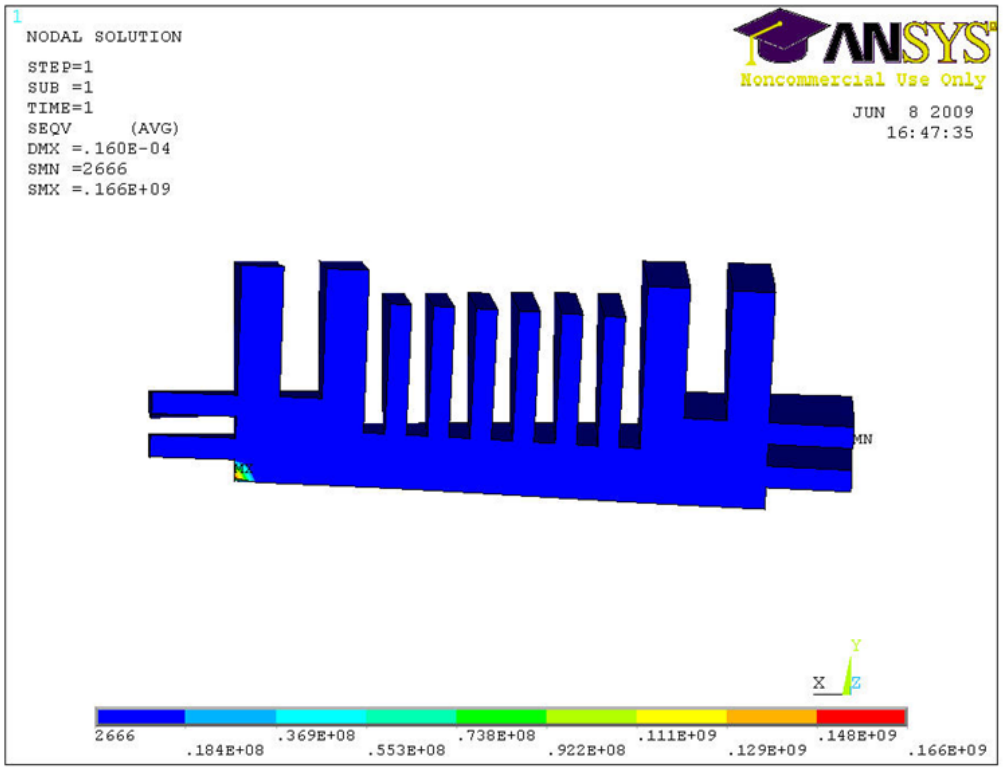

Figure 9-Static Analysis (back view)

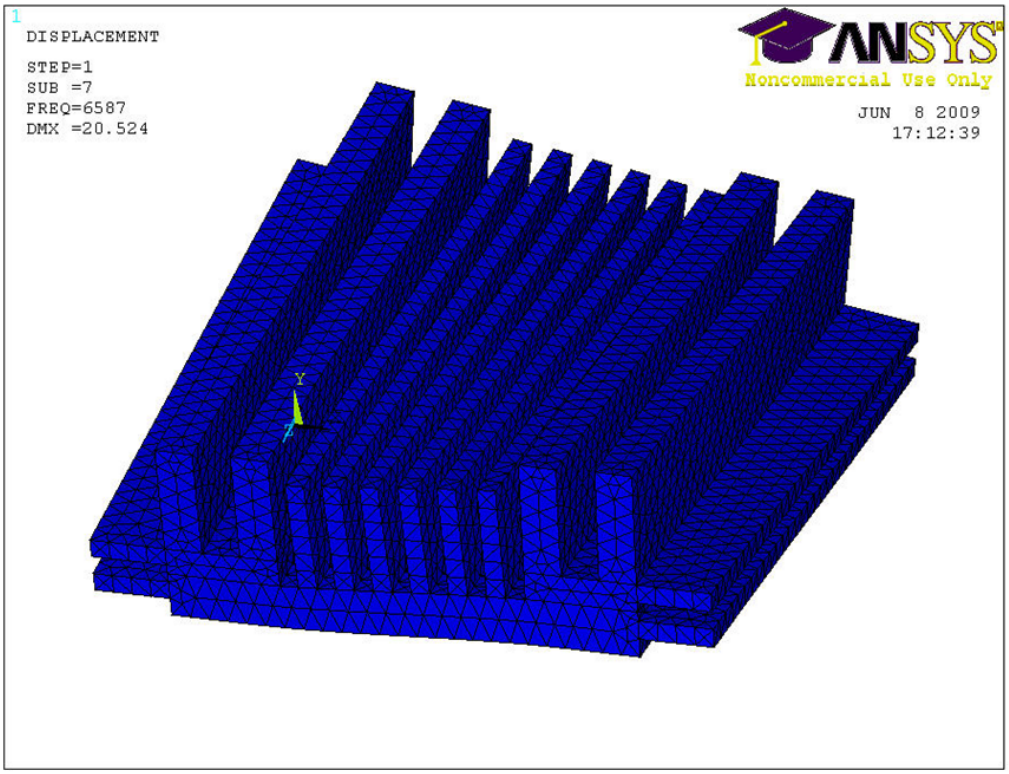

Figure 10-Mode 1

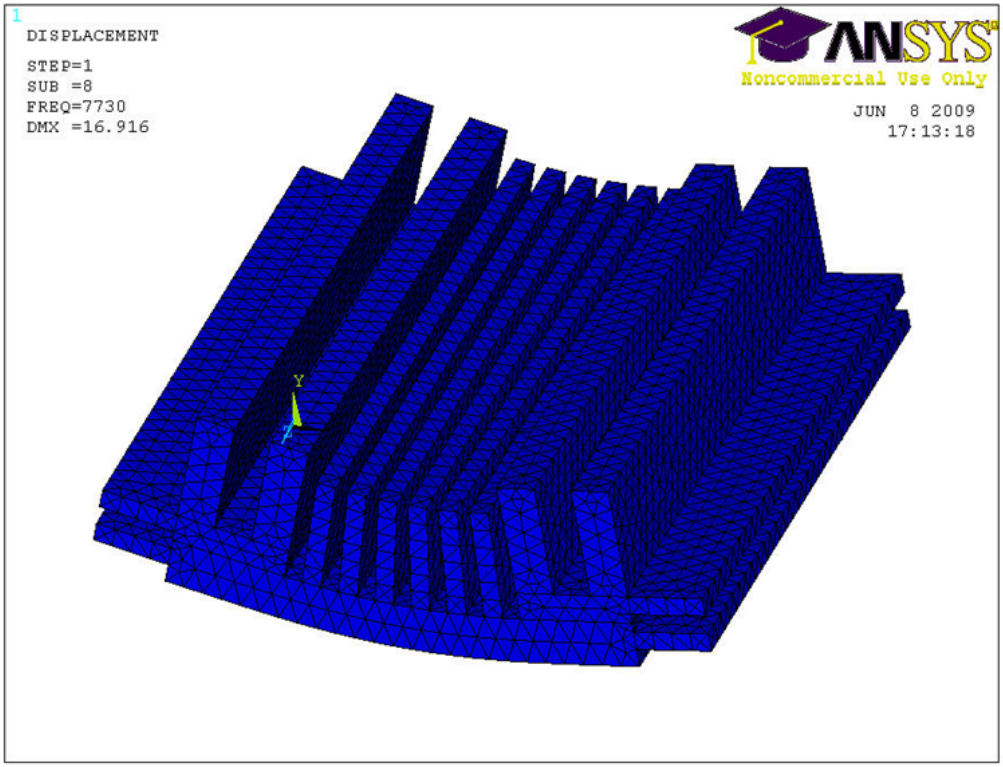

Figure 11-Mode 2

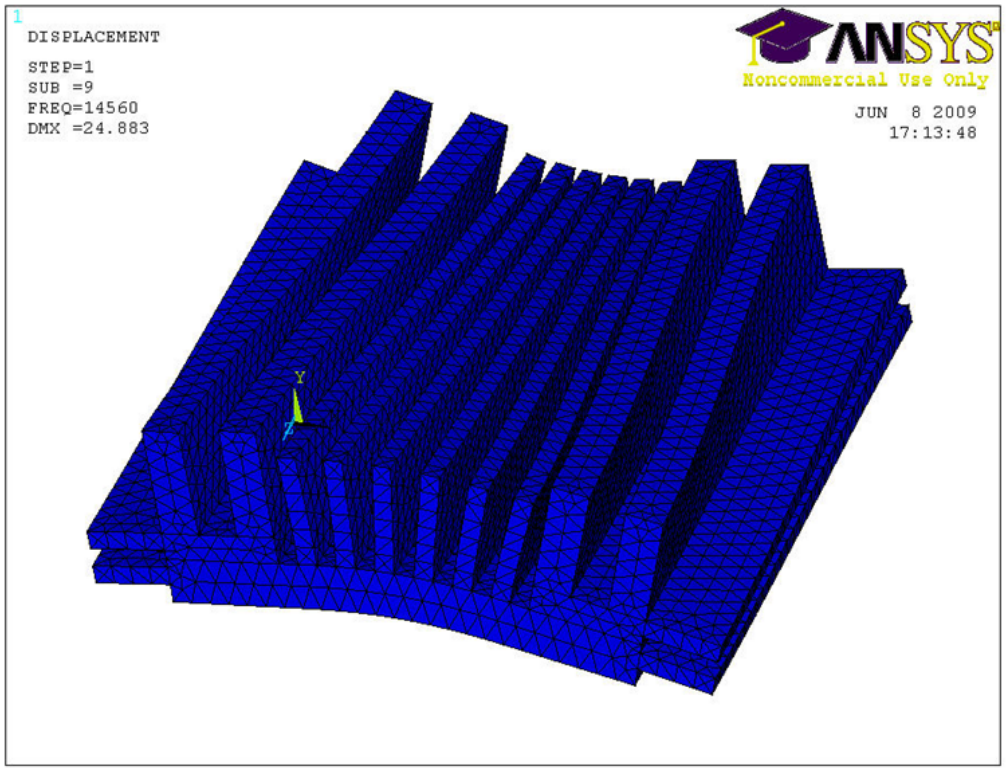

Figure 12-Mode 3

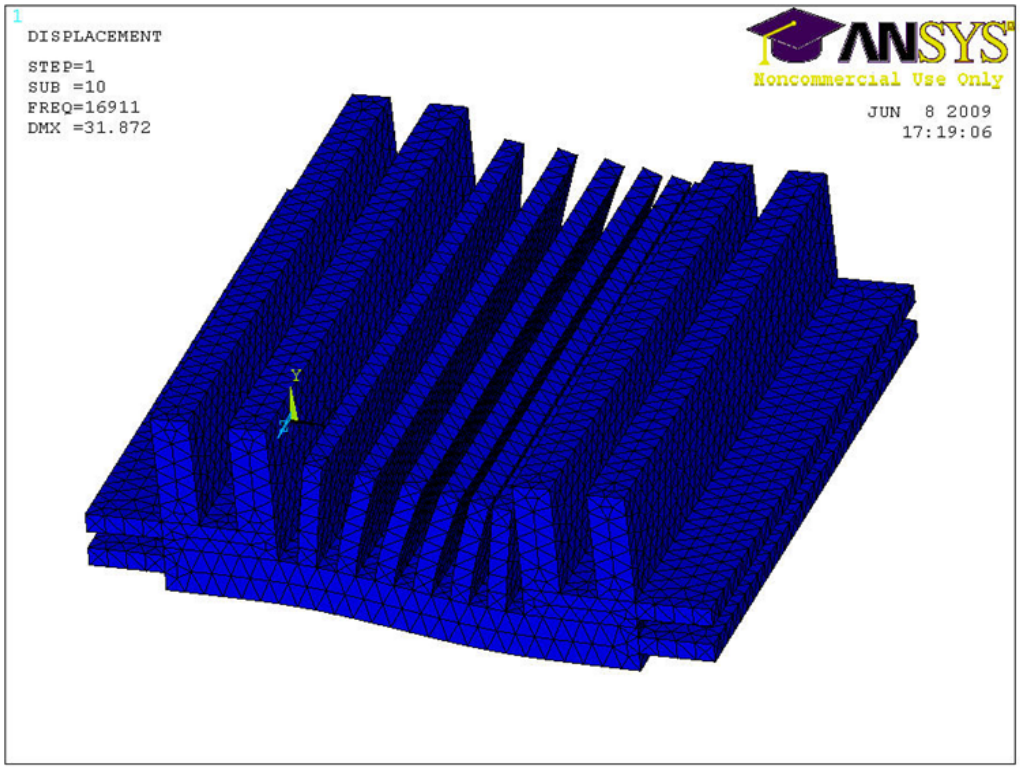

Figure 13-Mode 4

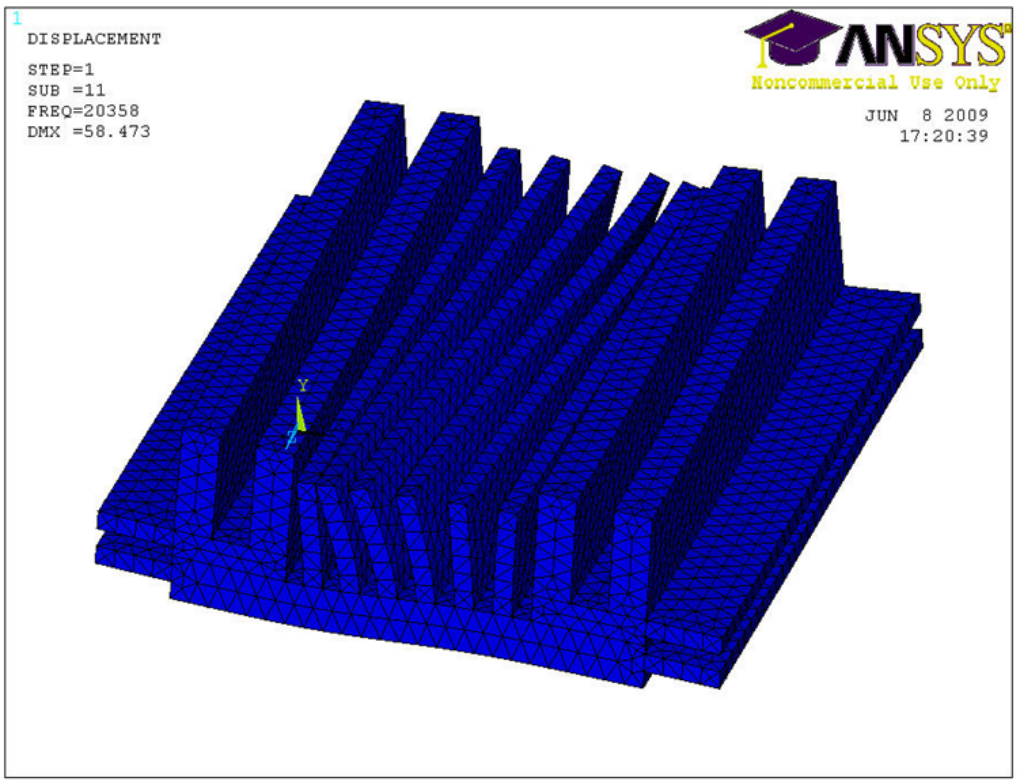

Figure 14-Mode 5

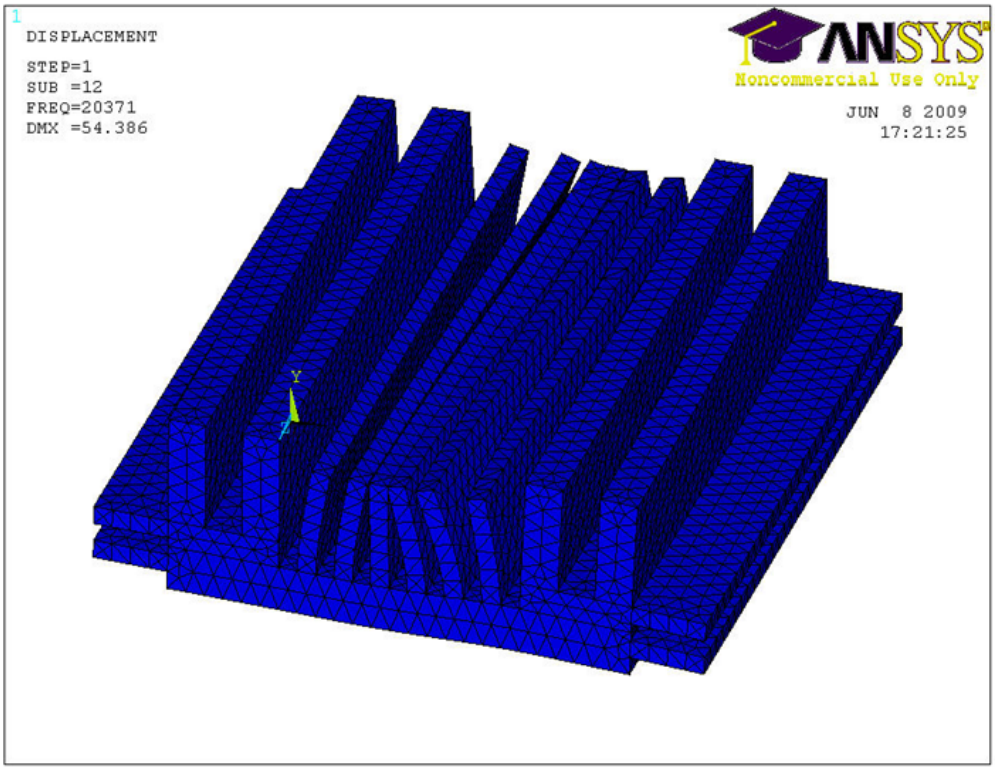

Figure 15-Mode 6

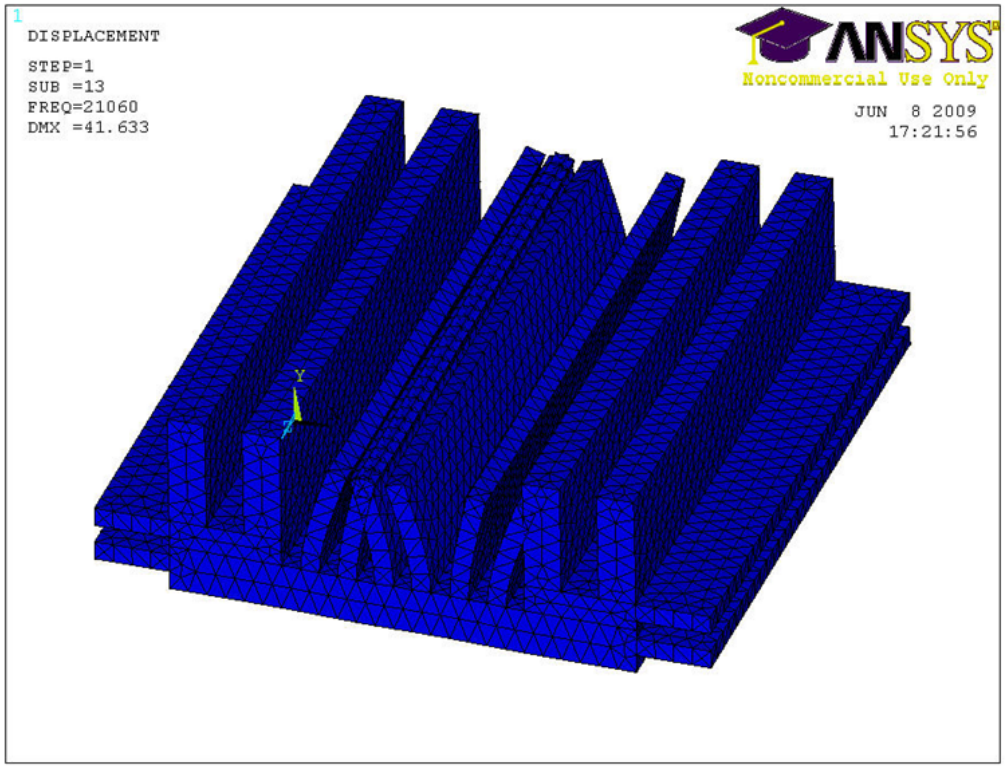

Figure 16-Mode 7

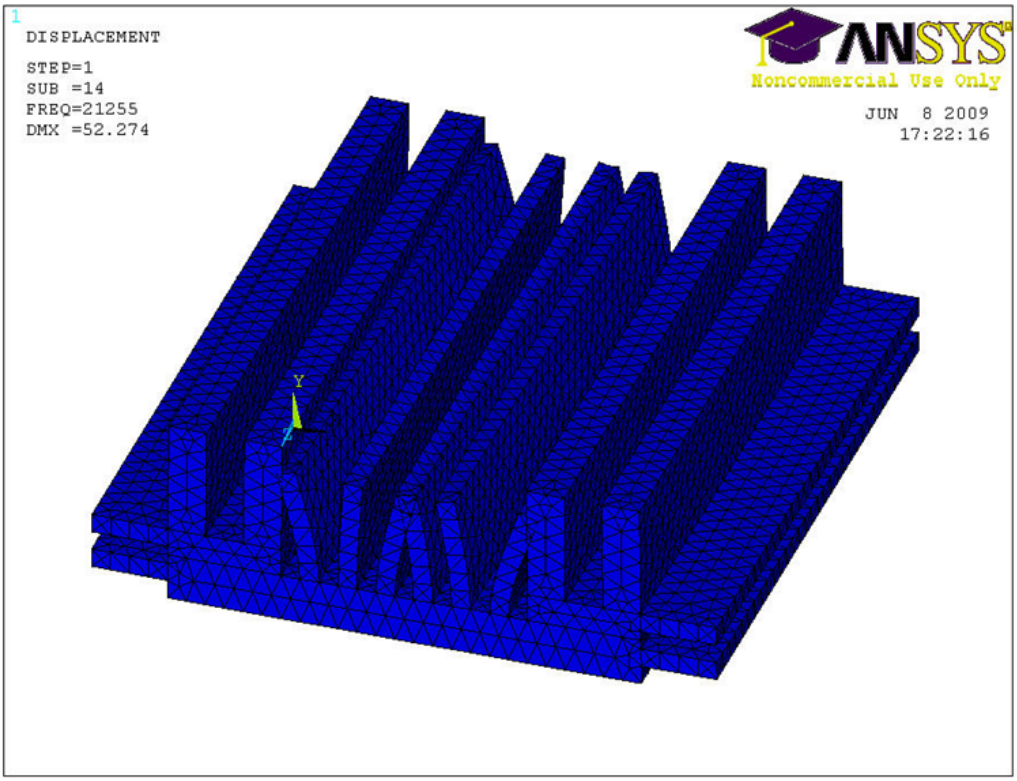

Figure 17-Mode 8

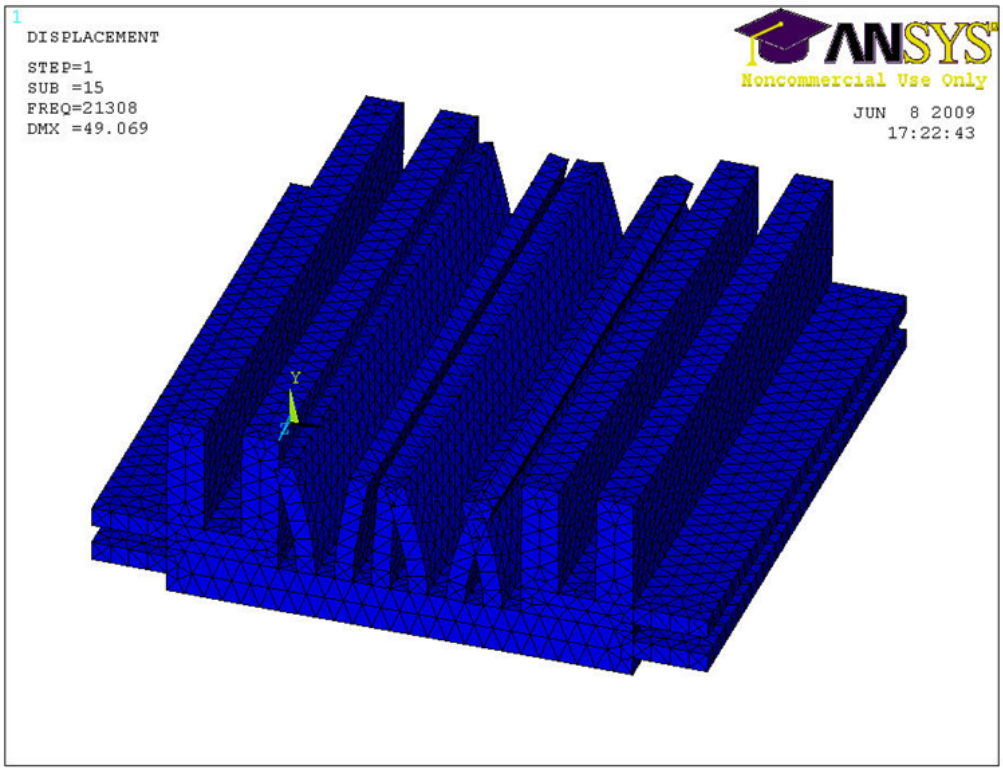

Figure 18-Mode 9

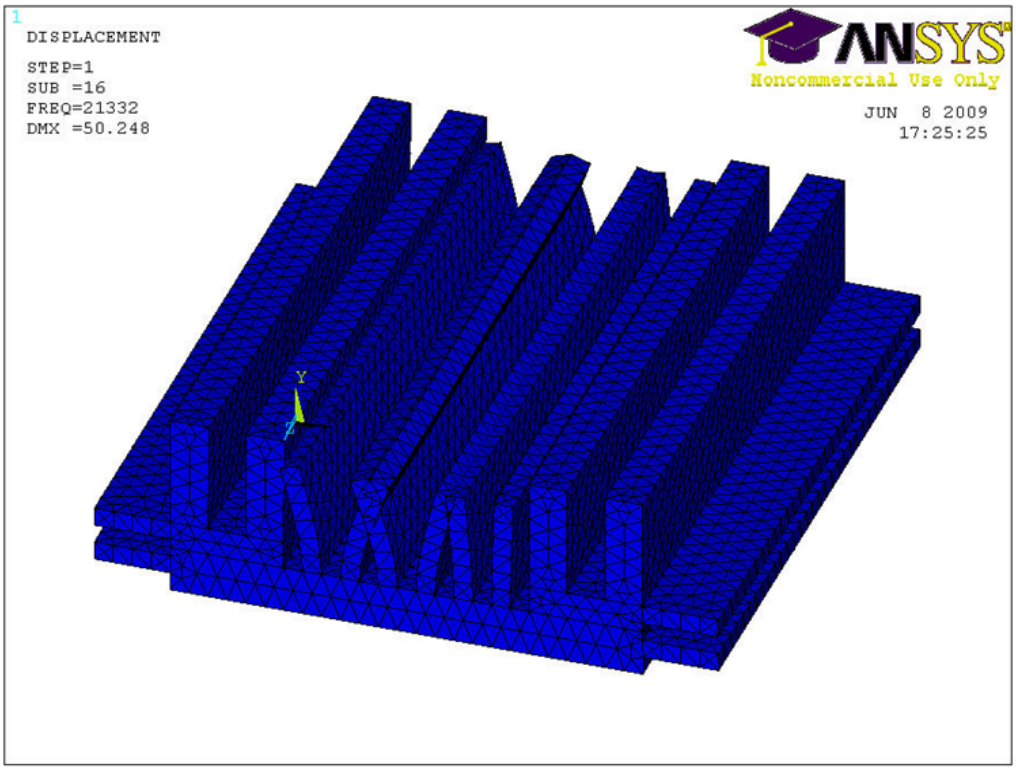

Figure 19-Mode 10